Electronics
Back-contact resistor network Pares wire count in ECL hybrids

Thin-film tantalum-nitride resistor chip eliminates four interior wire bonds with a common back contact

by Dieter Walter, Semi-films Division, National Micronetics Inc., West Hurley, N.Y., and Loyd Searle, High Tech Promotions, Inc. Woburn, Mass

□ Emitter-coupled-logic integrated circuits require dual-resistive-termination networks no matter how they are packaged. For some time now, printed-circuit users have been able to save space and simplify interconnections by availing themselves of the dual-termination networks built into single and dual in-line packages.

Hybrid manufacturers, on the other hand, have not had a chip component functionally similar to the DIP-based dual-terminator network. Now, a unique thin-film process has been designed exclusively for hybrid manufacturers, which emulates the simplicity of resistive networks in DIPS.

The dual-terminator back-contact resistor network for ICL hybrids is made from tantalum nitride, a resistor material that is self-passivating and impervious to moisture. The thin-film substrate is single-crystal silicon to ensure the best possible power dissipation characteristics. Back-contact technology reduces the number of bonding pads necessary and also obviates the need for interior wire bonding. Four ECL lines can be terminated with five bonds—a savings of four interior wire bonds.

All logic circuit interconnections are, inadvertently, transmission lines. As logic speeds and wiring lengths increase, reflections from the ends of the logic lines are more likely to interfere with the desired signals. The termination of a logic line with an appropriate resistive load, however, reduces these reflections.

A resistive divider consisting of two series resistors, R_H and R_L, forms a very practical terminator for ECL. The divider is connected between the positive and negative supply lines, and the logic line is connected to the divider output. Since the supply lines are electrically common to ac signals, the input impedance at the divider output is R_H in parallel with R_L. In addition, the divider functions like a pull-up or pull-down resistor. These terminators are called dual-terminating networks.

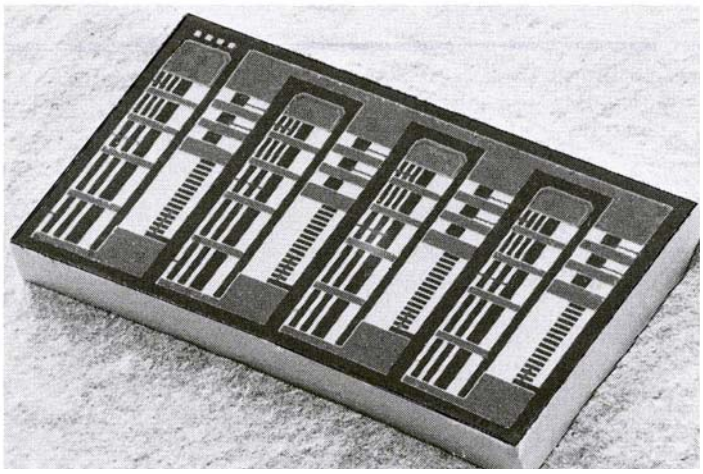
Wired at the back

The dual-terminator network sits on a 50-by-90-mil chip containing four terminator pairs (Fig. 1). Normally, four terminator chips with three pads each would have 12 pads requiring 12 wire bonds. Using common positive and negative buses on the chip would reduce the number of wire bonds to six, but would not significantly reduce the size of the chip. Also, all pads could not be located at the periphery of the chip. A more practical solution to the layout problem was achieved here by using back-contact technology.

Back-contact technology employs the silicon body of the chip as a circuit node. Heavily doped low-resistivity silicon is used to minimize parasitic resistances. The back of the wafer, and hence each chip, is metalized with gold. Electrical connections are made from the tantalum nitride film to the silicon body through etched windows in a silicon oxide layer. This technique has been used for many years to make single-resistor chips. With it, the user need make only one wire bond; the other connections are made through the die bond to the substrate.

The final design has one bus for the positive connections. This bus, employing aluminum metalization, runs along one edge of the chip (Fig. 2). It widens at four places to form bonding pads, any of which may be used. Along the opposite edge are locat5ed the four bonding pads for the logic lines. The metalization covering the back-contact windows appears as four "pads" in the interior of the chip. They are not intended for wire bonding since this bus is the back contact, which is bonded to a conductive pad on the final hybrid substrate.

Each resistor is of composite design—the is, each consists of several trimmable elements in series. This arrangement allows for wide trim ranges (up to 2:1), with a trim resolution of ≤ 2%, while limiting power dissipation density to 5,000 watts per



1. Back contact. A scanning electron microphotograph of the dual terminator for emitter-coupled-logic hybrid circuits shows the tantalum nitride resistors (the white areas) on a silicon substrate. The back contact of the chip is metalized with gold and connects to the resistors through windows in an insulating silicon dioxide layer.

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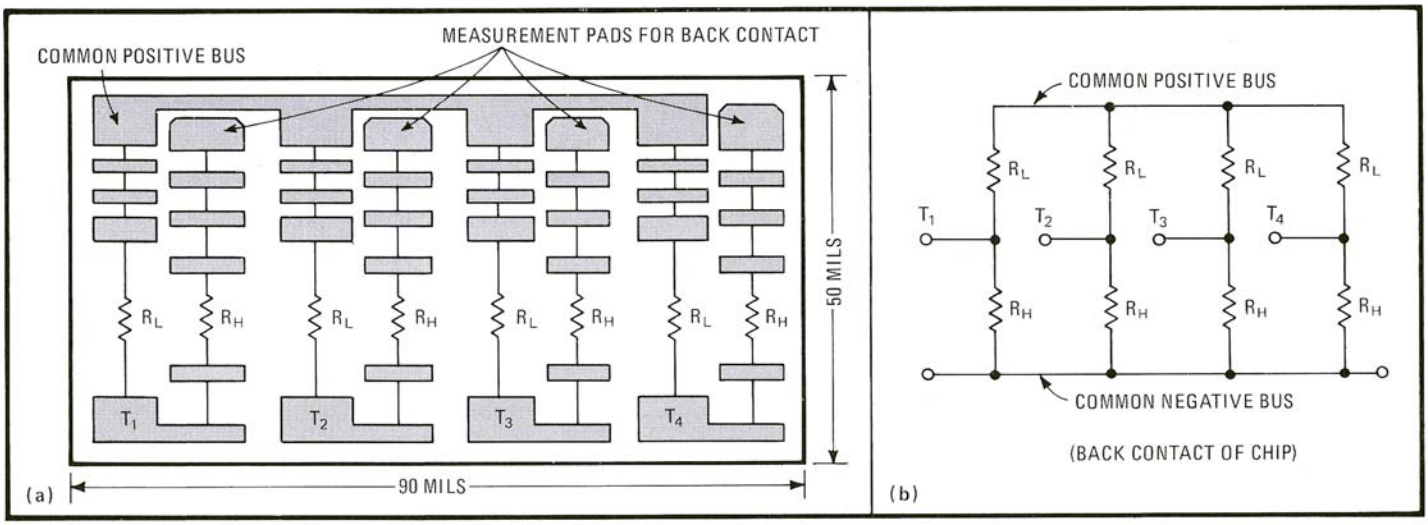

2. Saving bonds. Chip layout 9a) and equivalent circuit (b) of the emitter-coupled-logic terminator are depicted above. T_1, T_2, T_3, and T_4 are bonding pads for resistor junctions. The metalization of the chip's back forms the negative bus through the chip substrate.

square inch at any point in the film under worst-case conditions. The metalization bars separating the elements of each resistor contribute to the unique appearance of the chip.

On the wafer

In wafer form, direct electrical contact to the silicon body is not readily achieved. Instead, probes are placed on the back-contact pads as well as on the bonding pads. The equivalent circuits of the structure thus tested contain the eight desired tantalum nitride resistors, four undesired back-contact window resistances, and three resistances resulting from the bulk resistivity of the silicon. These 15 resistors are arranged in a circuit with three independent loops.

The parasitic resistances associated with the back contacts are low—several ohms or less—compared with 81 Ω and up for the terminator resistors. Each network must be tested to verify that the resistances are low enough. In wafer form, this is done by measuring the resistance between back-contact pads. However, because of low values, separate current and voltage probes must be used. Three of the four contact pads are too small to accept more than one probe. A solution is to use one probe for current and sense the voltage through one of the terminator resistors.

An additional complication arises from the fact that the terminator resistors shunt the parasitic resistances. The sensed voltage is therefore attenuated, and a true-ohms reading is not obtained. Nevertheless, it can be shown mathematically that a sufficiently accurate result is obtained by these measurements.

Multiple measurements

Measurement of the eight terminator resistors in closed-loop configuration is achieved by using an active guarding option available on the laser trimmer. This standard technique has to be slightly modified, again because of the inability to place more than one probe on the back-contact pad of the silicon wafer.

All the resistor networks on the chip are functionally tested in the same manner as any integrated circuit component. First, the chip is bonded to a conductive surface (ground) using conductive epoxy. The bus on the chip is then shorted to the ground surface, and the resistance measured between each logic terminator pad and ground. In this manner, dc measurements are used to predict as operation. The standard tolerance on the impedance is ± 2% and has been readily achieved by laser trimming with the previously discussed techniques.

Other samples are used to test for the output voltage, that is, the ration R_H (R_L+R_H). Again, the chips are bonded to a conductive surface. Two probes are used to apply a dc potential between the bus on the chip and the ground plane, and separate probes are used to measure the output voltage ratio. The 2% tolerance on the output voltage has been easily met by the manufacturing techniques described. The logic terminator chip is called upon to dissipate substantial power. For example, as a 50-Ω terminator for Signetics ECL II logic, the chip dissipated 636 milliwatts with nominal values and logical 1s applied.

Old reliable

Using tantalum nitride improves reliability; absolute resistance shift of the material ΔR/R is less than ±0.5%, after being tested to MIL-STD-202, Method 106 (moisture resistance). This is more representative of microelectronic operating environments than MIL-R-55342, since a bias is applied under high relative humidity. Method 106 consists of ten 16-hour cycles during which relative humidity and temperature are ramped up to 98% at 65° C and a bias equal to the working voltage is applied during the first 2 h of each 8-h half-cycle. IN addition, absolute resistance stability over 5,000 h at 125° C in air is ±0.2% maximum Δ R/R, while noise, tested to MIL-STD-202, Method 308, is rated at –35 decibels maximum. Under worst-case condition, power dissipation is limited to 5,000 W/in.^{2}

Experience with tantalum nitride's stability was used to select a conservative stability specification of less that 2% change in 1,000 h under load with a chip temperature not to exceed 125°C. Additional specifications, including temperature coefficient of resistance, high-temperature exposure, and thermal shock and moisture resistance, are par for tantalum nitride chip resistors. □